



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T133-500-10

Mean on-state current	I _{TAV}	500 A					
Repetitive peak off-state voltage	V _{DRM}	1000 V					
Repetitive peak reverse voltage	V _{RRM}						
Turn-off time	t _q	125, 160, 200, 250, 320, 400, 500 µs					
V _{DRM} , V _{RRM} , V	400	500	600	700	800	900	1000
Voltage code	4	5	6	7	8	9	10
T _j , °C				-60 ÷ 150			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I _{TAV}	Mean on-state current	A	500 875	T _c =120 °C, Double side cooled T _c =85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I _{TRMS}	RMS on-state current	A	785	T _c =120 °C, Double side cooled 180° half-sine wave; 50 Hz	
I _{TSM}	Surge on-state current	kA	10.0 12.0	T _j =T _j max T _j =25 °C 180° half-sine wave; 50 Hz (t _p =10 ms); single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 µs; di _G /dt≥1 A/µs	
			11.0 13.0	T _j =T _j max T _j =25 °C 180° half-sine wave; 60 Hz (t _p =8.3 ms); single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 µs; di _G /dt≥1 A/µs	
I ² t	Safety factor	A ² s·10 ³	500 720	T _j =T _j max T _j =25 °C 180° half-sine wave; 50 Hz (t _p =10 ms); single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 µs; di _G /dt≥1 A/µs	
			500 700	T _j =T _j max T _j =25 °C 180° half-sine wave; 60 Hz (t _p =8.3 ms); single pulse; V _D =V _R =0 V; Gate pulse: I _G =2 A; t _{GP} =50 µs; di _G /dt≥1 A/µs	
BLOCKING					
V _{DRM} , V _{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	400÷1000	T _{j min} < T _j < T _{j max} ; 180° half-sine wave; 50 Hz; Gate open	
V _{DSM} , V _{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	500÷1100	T _{j min} < T _j < T _{j max} ; 180° half-sine wave; 50 Hz;single pulse; Gate open	
V _D , V _R	Direct off-state and Direct reverse voltages	V	0.75·V _{DRM} 0.75·V _{RRM}	T _j =T _j max; Gate open	

TRIGGERING				
I _{FGM}	Peak forward gate current	A	6	T _j =T _j max
V _{RGM}	Peak reverse gate voltage	V	5	
P _G	Gate power dissipation	W	3	T _j =T _j max for DC gate current
SWITCHING				
(di _T /dt) _{crit}	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	320	T _j =T _j max; V _D =0.67·V _{DRM} ; I _{TM} =2 I _{TAV} ; Gate pulse: I _G =2 A; t _{GP} =50 μ s; di _G /dt≥1 A/ μ s
THERMAL				
T _{stg}	Storage temperature	°C	-60÷50	
T _j	Operating junction temperature	°C	-60÷150	
MECHANICAL				
F	Mounting force	kN	9.0÷11.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped
CHARACTERISTICS				
Symbols and parameters		Units	Values	Conditions
ON-STATE				
V _{TM}	Peak on-state voltage, max	V	1.50	T _j =25 °C; I _{TM} =1570 A
V _{T(TO)}	On-state threshold voltage, max	V	0.95	T _j =T _j max;
r _T	On-state slope resistance, max	mΩ	0.420	0.5 π I _{TAV} < I _T < 1.5 π I _{TAV}
I _L	Latching current, max	mA	700	T _j =25 °C; V _D =12 V; Gate pulse: I _G =2 A; t _{GP} =50 μ s; di _G /dt≥1 A/ μ s
I _H	Holding current, max	mA	300	T _j =25 °C; V _D =12 V; Gate open
BLOCKING				
I _{DRM} , I _{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	T _j =T _j max; V _D =V _{DRM} ; V _R =V _{RRM}
(dv _D /dt) _{crit}	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000	T _j =T _j max; V _D =0.67V _{DRM} ; Gate open
TRIGGERING				
V _{GT}	Gate trigger direct voltage, max	V	4.00 2.50 2.00	T _j = T _j min T _j =25 °C T _j = T _j max
I _{GT}	Gate trigger direct current, max	mA	400 250 200	T _j = T _j min T _j = 25 °C T _j = T _j max
V _{GD}	Gate non-trigger direct voltage, min	V	0.25	T _j =T _j max; V _D =0.67V _{DRM} ;
I _{GD}	Gate non-trigger direct current, min	mA	10.00	Direct gate current
SWITCHING				
t _{gd}	Delay time	μ s	2.00	T _j =25 °C; V _D =0.4V _{DRM} ; I _{TM} =I _{TAV} ; Gate pulse: I _G =2 A; t _{GP} =50 μ s; di _G /dt≥1 A/ μ s
t _q	Turn-off time ²⁾ , max	μ s	125, 160, 200, 250, 320, 400, 500	dv _D /dt=50 V/ μ s; T _j =T _j max; I _{TM} = I _{TAV} ; di _R /dt=-10 A/ μ s; V _R =100V; V _D =0.67V _{DRM}

THERMAL						
R_{thjc}	Thermal resistance, junction to case, max	$^{\circ}\text{C}/\text{W}$	0.040	Direct current	Double side cooled	
R_{thjc-A}			0.088		Anode side cooled	
R_{thjc-K}			0.072		Cathode side cooled	
R_{thck}	Thermal resistance, case to heatsink, max	$^{\circ}\text{C}/\text{W}$	0.008	Direct current		

MECHANICAL						
W	Weight, typ	g	110			
D_s	Surface creepage distance	mm (inch)	10.30 (0.405)			
D_a	Air strike distance	mm (inch)	6.30 (0.248)			

PART NUMBERING GUIDE							NOTES					
T	133	500	10	A2	X2	N						
1	2	3	4	5	6	5						
1. Phase Control Thyristor												
2. Design version												
3. Mean on-state current, A												
4. Voltage code												
5. Critical rate of rise of on-state current non-repetitive, $\text{V}/\mu\text{s}$												
6. Turn-off time ($\text{dv}_D/\text{dt}=50 \text{ V}/\mu\text{s}$)												
7. Ambient conditions: N – normal; T – tropical												

Symbol of Group P2 K2 E2 A2

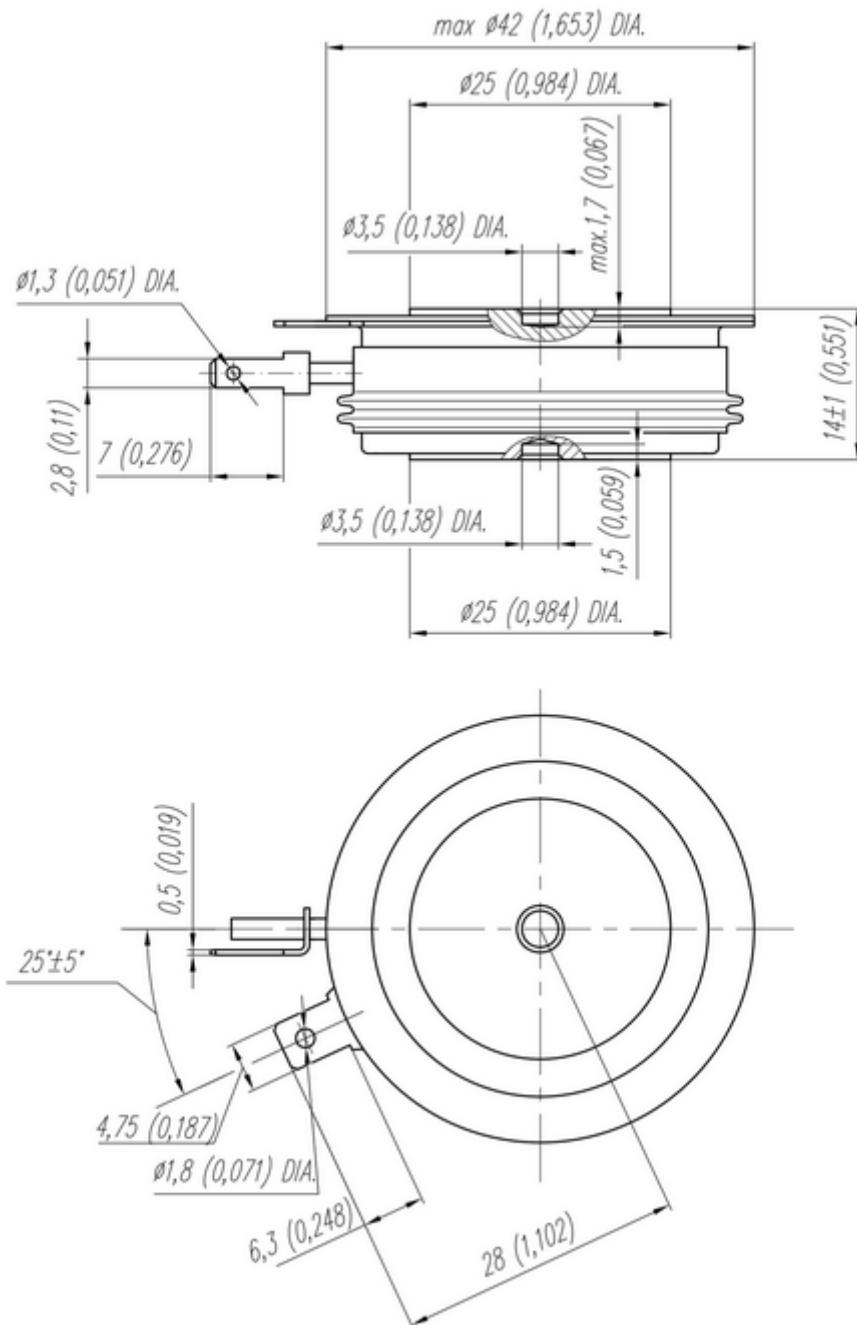
(dv_D/dt)_{crit}, $\text{V}/\mu\text{s}$ 200 320 500 1000

Symbol of Group X2 T2 P2 M2 K2 H2 E2

$t_{q, \mu\text{s}}$ 125 160 200 250 320 400 500

OVERALL DIMENSIONS

Package type: T.B2



All dimensions in millimeters (inches)

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